

# PMK35EP

P-channel TrenchMOS extremely low level FET

Rev. 01 — 17 September 2007

Product data sheet

## 1. Product profile

### 1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Low threshold voltage
- Low  $R_{DSon}$

### 1.3 Applications

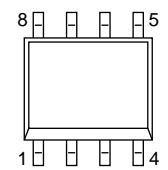
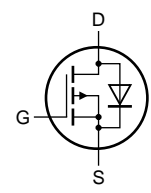
- Load switching
- Battery management

### 1.4 Quick reference data

- $V_{DS} \leq -30$  V
- $I_D \leq -14.9$  A
- $R_{DSon} \leq 19$  m $\Omega$
- $Q_{GD} = 6$  nC (typ)

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)	 SOT96-1 (SO8)	 001aaa025
4	gate (G)		
5, 6, 7, 8	drain (D)		

### 3. Ordering information

**Table 2. Ordering information**

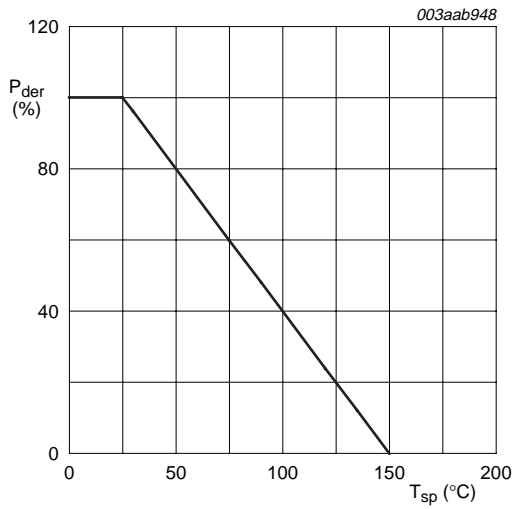
Type number	Package		Version
	Name	Description	
PMK35EP	SO8	SO8: plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

### 4. Limiting values

**Table 3. Limiting values**

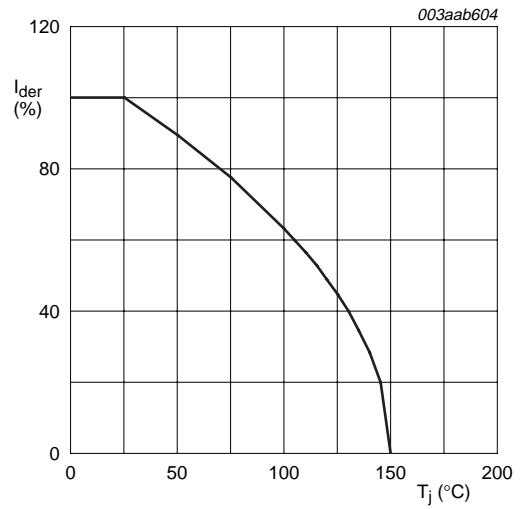
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-30	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	-30	V
$V_{GS}$	gate-source voltage		-	$\pm 25$	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = -10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	-14.9	A
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = -10\text{ V}$ ; see <a href="#">Figure 2</a>	-	-7	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	-28.8	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	6.9	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ °C}$	-	-5.8	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	-23	A



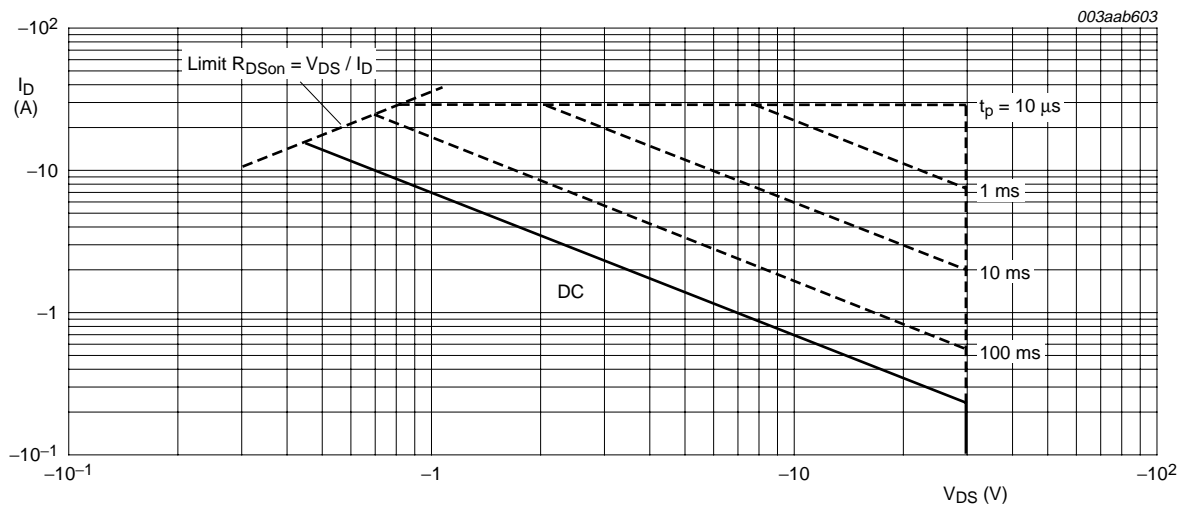
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{sp} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	18	K/W

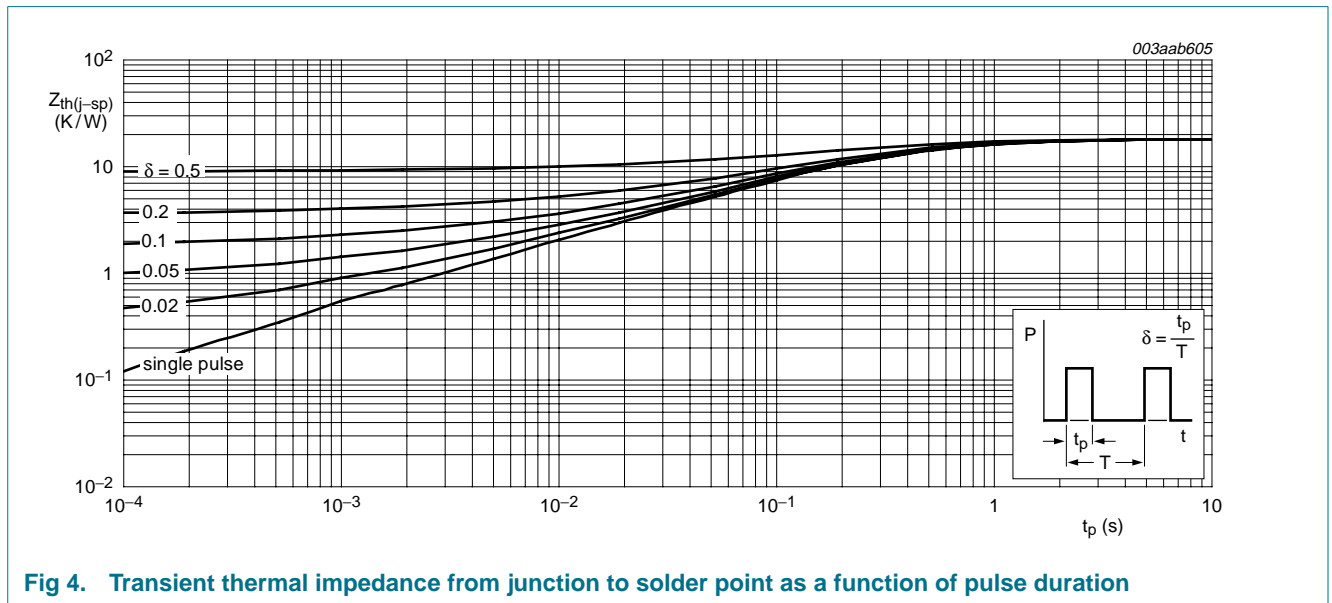


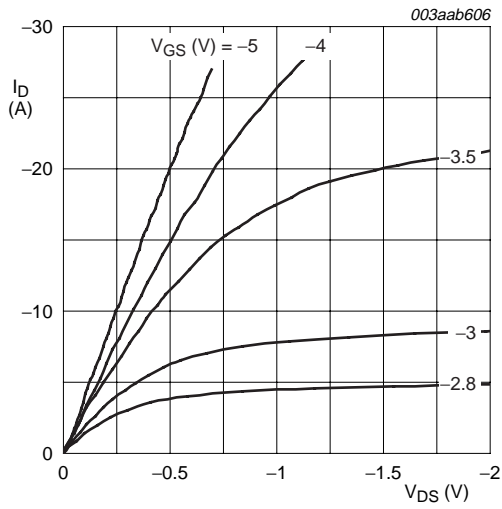
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

**Table 5. Characteristics**

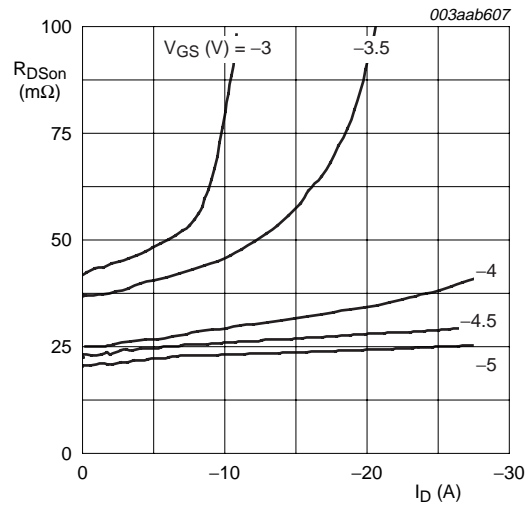
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-30	-	-	V
		$T_j = -55\text{ °C}$	-27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -250\ \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a> $T_j = 25\text{ °C}$	-1	-	-3	V
		$T_j = 150\text{ °C}$	-0.7	-	-	V
		$T_j = -55\text{ °C}$	-	-	-3.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = -30\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	-	-1	$\mu\text{A}$
		$T_j = 70\text{ °C}$	-	-	-10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\ \text{V}$ ; $V_{DS} = 0\ \text{V}$	-	-	-100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\ \text{V}$ ; $I_D = -9.2\ \text{A}$ ; see <a href="#">Figure 8</a> $T_j = 25\text{ °C}$	-	16	19	m $\Omega$
		$T_j = 150\text{ °C}$	-	25	31	m $\Omega$
		$V_{GS} = -4.5\ \text{V}$ ; $I_D = -6.8\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	26	35	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = -9.2\ \text{A}$ ; $V_{DS} = -15\ \text{V}$ ; $V_{GS} = -10\ \text{V}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	42	-	nC
$Q_{GS}$	gate-source charge		-	8	-	nC
$Q_{GD}$	gate-drain charge		-	6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	-2.5	-	V
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}$ ; $V_{DS} = -25\ \text{V}$ ; $f = 1\ \text{MHz}$ ; see <a href="#">Figure 14</a>	-	2100	-	pF
$C_{oss}$	output capacitance		-	365	-	pF
$C_{rSS}$	reverse transfer capacitance		-	275	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15\ \text{V}$ ; $R_L = 6\ \Omega$ ; $V_{GS} = -10\ \text{V}$ ; $R_G = 6\ \Omega$	-	9	-	ns
$t_r$	rise time		-	9	-	ns
$t_{d(off)}$	turn-off delay time		-	50	-	ns
$t_f$	fall time		-	24	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -3.45\ \text{A}$ ; $V_{GS} = 0\ \text{V}$ ; see <a href="#">Figure 13</a>	-	-0.8	-1.2	V



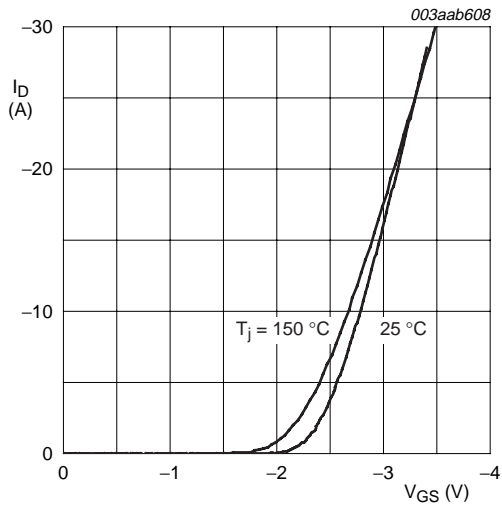
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



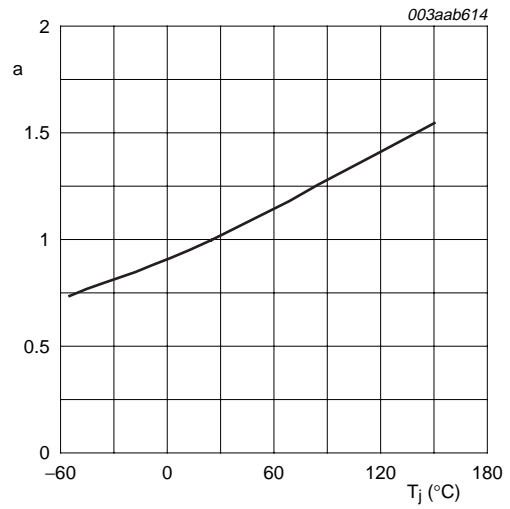
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



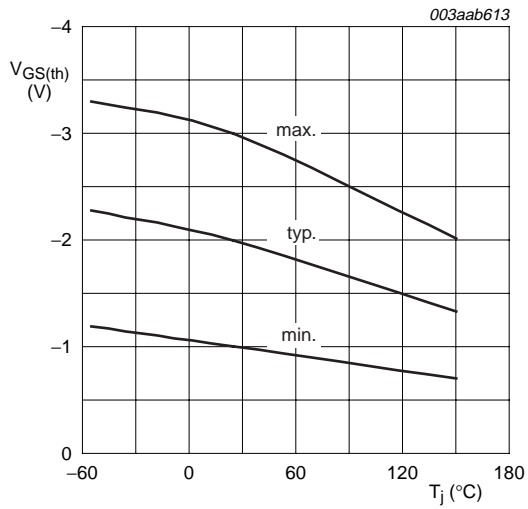
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



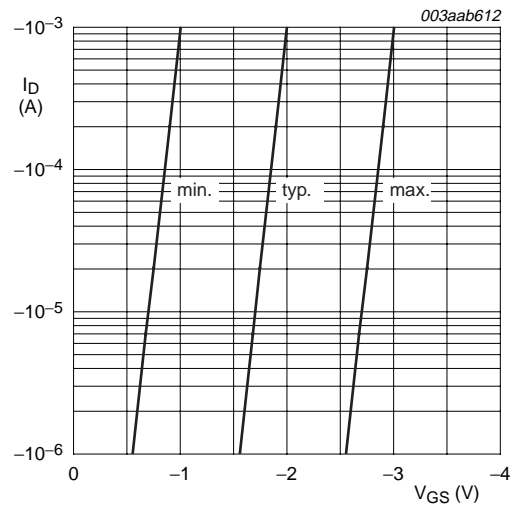
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



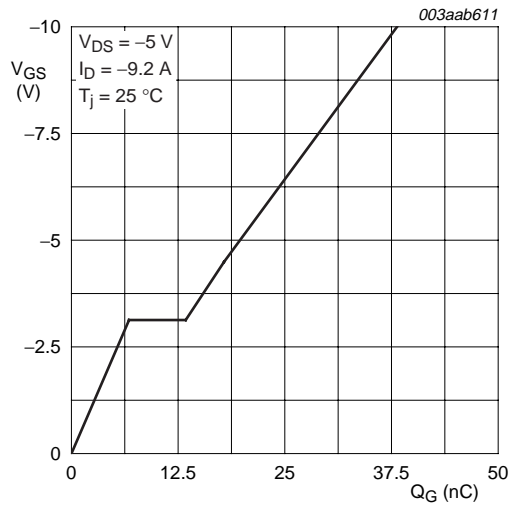
$I_D = -1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^{\circ}C; V_{DS} = -5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = -9.2 \text{ A}; V_{DS} = -15 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

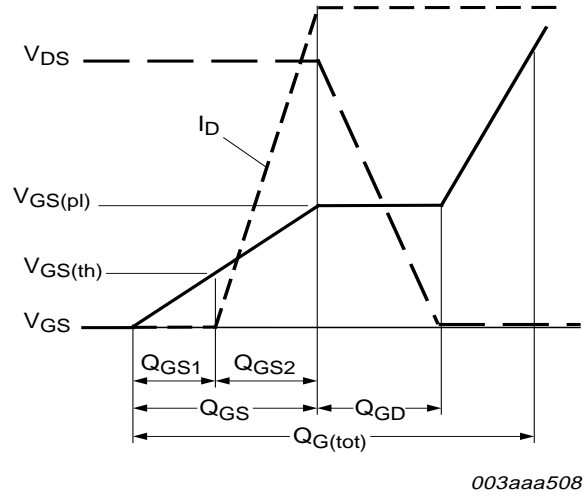
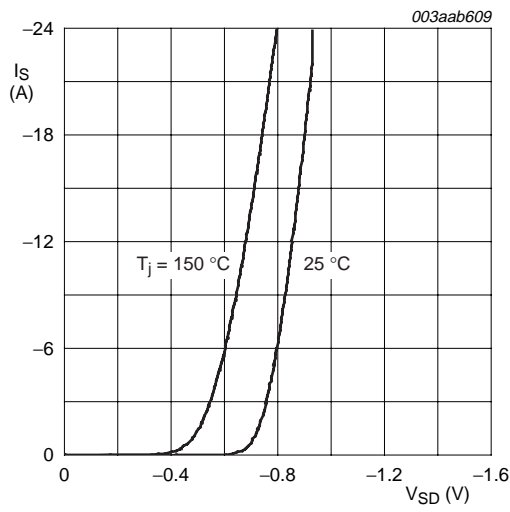
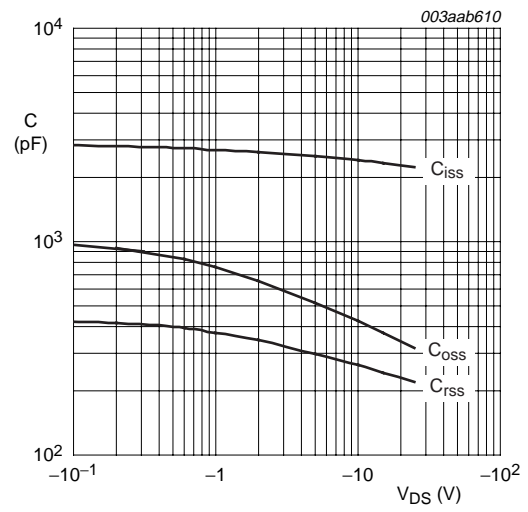


Fig 12. Gate charge waveform definitions



$T_j = 25\text{ °C}$  and  $150\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

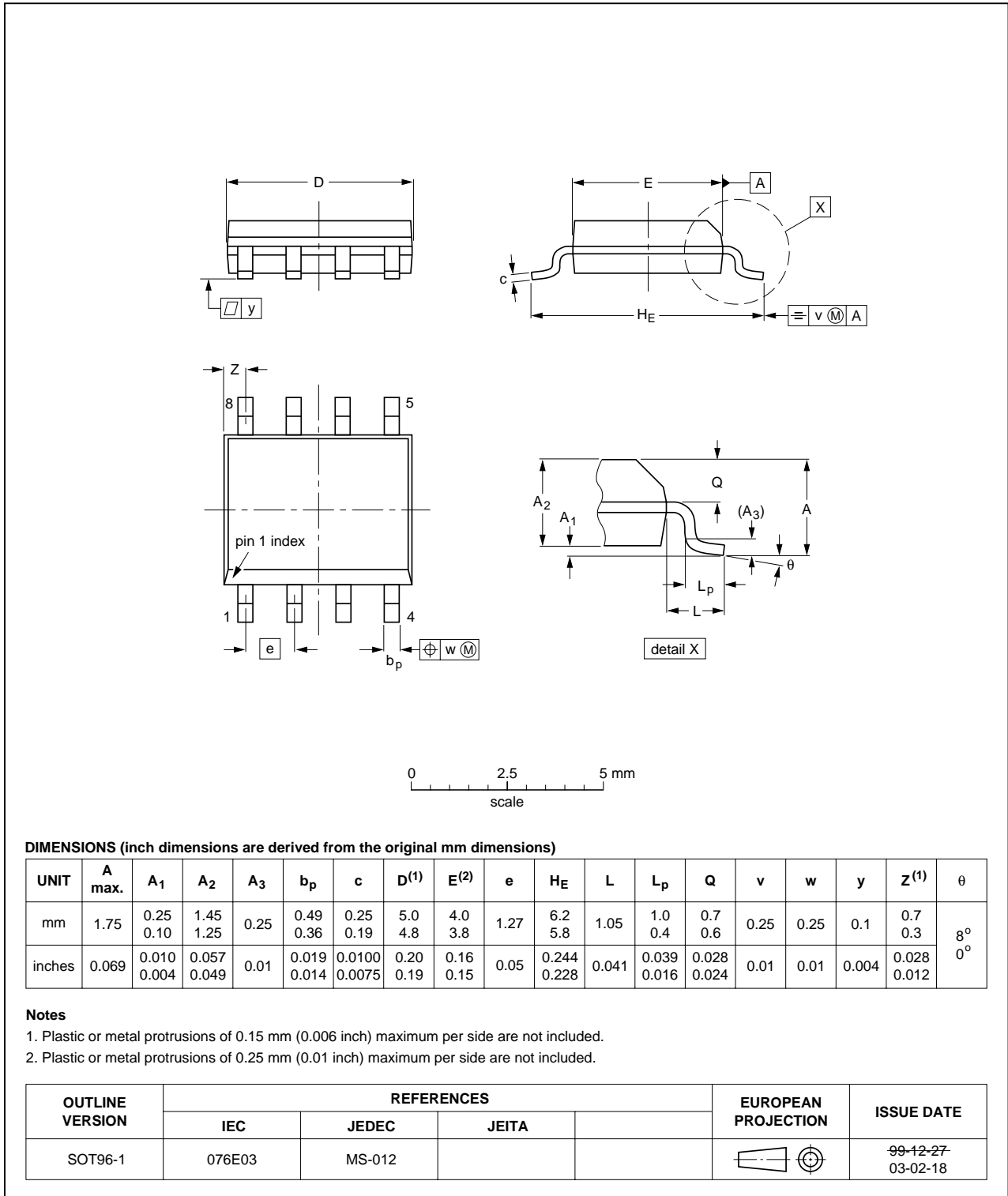


Fig 15. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMK35EP_1	20070917	Product data sheet	-	-

## 9. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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